

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT: FRANCO MOTIKA ET AL.

FOR: SYSTEM AND METHOD FOR TESTING
ELECTRONIC DEVICES ON A MICROCHIP

INFORMATION DISCLOSURE STATEMENT
UNDER 37 CFR §§ 1.56, 1.97 AND 1.98

The Commissioner of Patents
and Trademarks
P.O. Box 1450
Alexandria, VA 22313-1450

In compliance with the duty to disclose, applicants submit herewith a copy of each publication, excluding U.S. Patents and U.S. published patent applications, of which those designated by 37 CFR § 1.56 are aware; the publications are listed on attached form PTO-1449. The present Information Disclosure Statement shall not be construed as a representation that a search has been made or that no other art than that identified on the attached form PTO-1449 exists.

Consideration of this Information Disclosure Statement is respectfully requested, since the Examiner may consider the information provided herein material to the patentability of the subject application as defined in 37 CFR § 1.56.

Since this Information Disclosure Statement is being filed within three months of the filing date of the subject application, no fee or certification under 37 CFR § 1.97 (e) is

POU920030178US1


required.

However, in the event the Commissioner of Patents deems that any fee is required under 37 CFR §§ 1.16 and 1.17 in connection with this application, applicants' attorneys authorize that such fee be charged to Deposit Account No. 09-0463.

Respectfully submitted,

FRANCO MOTIKA ET AL.

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INFORMATION DISCLOSURE CITATION <i>(Use several sheets if necessary)</i>	Docket Number (Optional) POU920030178US1	Application Number NYA
	Applicant(s) Motika, et al.	
	Filing Date NYA	Group Art Unit NYA

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	1	3,761,695	09-25-1973	Eichelberger	235	153	08-16-1972
	2	4,503,537	03-05-1985	McAnney	371	25	11-08-1982
	3	4,513,418	04-23-1985	Bardell et al.	371	25	11-08-1982
	4	4,598,401	07-01-1986	Whelan	371	25	06-25-1984
	5	4,726,025	02-16-1988	Splett et al.	371	25	10-16-1985
	6	4,893,072	01-09-1990	Matsumoto	371	223	06-22-1988
	7	5,528,602	06-18-1996	West et al.	371	22.4	03-09-1995
	8	5,983,380	11-09-1999	Motika et al.	714	733	09-16-1997
	9	6,311,311B1	10-30-2001	Swaney et al.	716	4	08-19-1999
	10	6,401,226B1	06-04-2002	Maeno	714	728	07-08-1999
	11	6,442,723B1	08-27-2002	Koprowski et al.	714	732	05-12-1999

FOREIGN PATENT DOCUMENTS

REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
						YES	NO
12	JP8005711A	1996-01-12	Japan	G01R31	28		✓

OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*

		W.H. Mcanney and J. Savir, "Built-In Checking of the Correct Self-Test Signature", September 1988, IEEE Transactions on Computers, Vol., 37, No. 9, pp. 1142-1145
		J. Savir and William H. McAnney, "A Multiple Seed Linear Feedback Shift Register", February 1992, IEEE Transactions on Computers, Vol. 41, No. 2, pp. 250-252

EXAMINER	DATE CONSIDERED
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EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP Section 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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		Bernd Konemann, Joachim Mucha and Gunther Zwiehoff, "Built-In Test for Complex Digital Integrated Circuits", June 1980, IEEE Journal of Solid State Circuits, Vol. SC-15, No. 3, pp. 315-319.			
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